

SELF-TIMED READ AND WRITE**ASSIST AND RESTORE CIRCUIT****ABSTRACT OF THE DISCLOSURE**

5 A read and write assist and restore circuit for a
memory device includes a first device, which is responsive
to a potential on a bit line such that the potential on the
bit line activates the first device. A second device is
driven by the first device such that when the first device
10 is activated, a change in the bit line potential is
reinforced with positive feedback by the second device
during a wordline active period to enable write-back of
data lost as a result of threshold voltage fluctuations in
memory cell transistors coupled to the bit line.

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